

SPICE Device Model SUM85N03-06P

Vishay Siliconix

N-Channel 30-V (D-S) 175° MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- · Macro Model (Subcircuit Model)
- Level 3 MOS

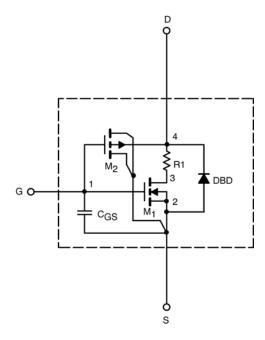
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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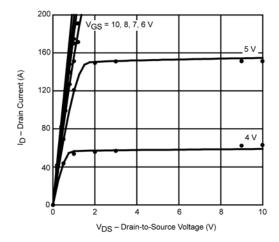
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	-				-
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.8		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	923		Α
Drain-Source On-State Resistance ^a	Γ _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	0.0044	0.0053	Ω
		V_{GS} = 10 V, I_{D} = 20 A, T_{J} = 125°C	0.008		
		V _{GS} = 4.5 V, I _D = 20 A	0.0077	0.0078	
Forward Voltage ^a	V_{SD}	I _S = 100 A, V _{GS} = 0 V	0.89	1.2	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	3135	3100	pF
Output Capacitance	C _{oss}		509	565	
Reverse Transfer Capacitance	C _{rss}		177	255	
Total Gate Charge ^c	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 50 A	47	48	nC
Gate-Source Charge ^c	Q_{gs}		10	10	
Gate-Drain Charge ^c	Q_{gd}		7.5	7.5	
Turn-On Delay Time ^c	t _{d(on)}	V_{DD} = 15 V, R_{L} = 0.30 Ω $I_{D} \cong 50$ A, V_{GEN} = 10 V, R_{G} = 2.5 Ω I_{F} = 50 A, di/dt = 100 A/ μ s	10	12	ns
Rise Time ^c	t _r		14	12	
Turn-Off Delay Time ^c	t _{d(off)}		26	30	
Fall Time ^c	t _f		33	10	
Source-Drain Reverse Recovery Time	t _{rr}		31	35	

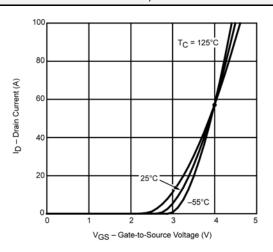
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.

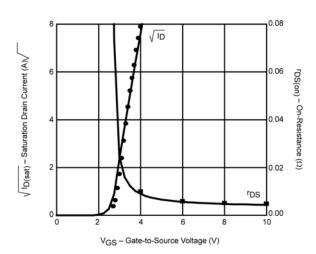


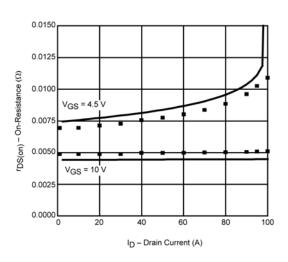
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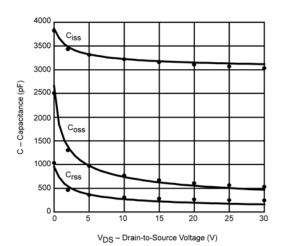
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

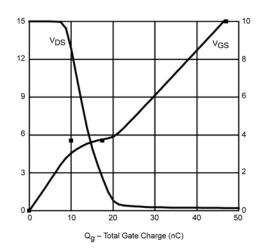












Note: Dots and squares represent measured data.



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